

ABSTRACT

A memory system includes a memory cache responsive to a single processing unit. The memory cache is arrangeable to include a first independently cached area assigned to store a first number of data packets based on a first processing unit context, and a second independently cached area assigned to store a second number of data packets based on a second processing unit context. A memory control system is coupled to the memory cache, and is configured to arrange the first independently cached area and the second independently cached area in such a manner that the first number of data packets and the second number of data packets coexist in the memory cache and are available for transfer between the memory cache and the single processing unit.